Page 221, replace line 9 as follows:--surface 7407 of a rectangular interface board, and the output switching elements are--.

A2

Page 222, replace line 2 as follows:--realization of a "fiber-array package". Each I/O switching element in a fiber-array--.

A3

Page 223, add after line 1:--Once a PCB is resulted from a step of PCB implementation, it cannot be used in another step of PCB implementation, and the same for the IC chip.--.

A4

Page 224, replace line 9 as follows:--construction and is not implemented in any of the aforementioned levels. Such a--.

A5

Page 233, replace line 9 as follows:--node by 2^d lines. In this case, $D=2^d$ where D is the scale-down factor. The parameter d is called the "scale-down exponent".--.

A6

Page 233, replace line 17 as follows:--2^{n-r} $2^r \times 2^r$ output nodes, the interstage exchange is induced by a permutation σ on integers--.

A7

Page 234, replace lines 17-18 as follows:--r+1−d to 1, r+2−d to 2, … , n−2d to n−r−d, and hence the interstage exchange is the 2^d-line version of the $(r-d)^{th}$ power of the $2^{n-2d} \times 2^{n-2d}$ shuffle exchange $SHUF^{(n-2d)}$. This is referred to as the "default choice" for π in this context.--.

A8 A9

Page 235, replace line 2 as follows:--2^d-line version of the exchange $SWAP^{(n-2d,\, r-d)}$.--.

A9

Page 235, replace line 14 as follows:--employ the modified 2-stage interconnection, the resulting network is not a--.

A10

Page 236, replace lines 2-3 as follows:-- essence, when one or more of the recursive steps in the recursive application of bit-permuting 2-stage interconnection

A11

A11 employ the modified 2-stage interconnection, the resulting network is routable. Therefore, the self-routing mechanism for the--.

Page 236, replace lines 14-16 as follows: --routing tag $D_{\gamma(p)}$ is equal to the q-th symbol $D_{\gamma(q)}$, where p<q, the whole stage of switching nodes at either stage-p or stage-q can be disabled.--.

A12

Page 237, replace lines 6-7 as follows: --routing tag are distinct.--.

Page 240, replace lines 11-12 as follows: --Therefore, when applying the modified 2-stage interconnection, there are D units of interconnection lines between any pair of input node and output node, where D is the scale-down factor, so this arrangement--.

A13

Page 240, replace lines 17-18 as follows: --one way to accommodate this is to add a small adaptor to each D units of lines of each input node and each output node. This method is especially convenient when D is not too large--.

A14

Page 241, replace line 1 as follows: --and the D units of lines connecting each pair of input node and output node are neighboring--.

Page 241, replace line 2 as follows: --to each other. The following is such an example with D=2. FIG. 79A is the planar--.

Page 241, replace lines 5-6 as follows: --respectively represent an 8-unit-in-8-unit-out PCB, and as D=2, each input node is connected to each output node by 2 units of interconnection lines (**7903**), resulting--.

Page 242, replace line 15 as follows: --each of the input switching nodes and/or an input exchange should be prepended to each of--.